STIC Search Report
EIC 2100

USPTO

STIC Database Tracking Number: 121187

TO: John Tabone **Location: 6B05** **Art Unit : 2133** **Wednesday, May 05, 2004** **Case Serial Number: 09/876753**	**From: David Holloway** **Location: EIC 2100** **PK2-4B30** **Phone: 308-7794** **david.holloway@uspto.gov**

Search Notes

Dear Examiner Tabone,

Attached please find your search results for above-referenced case.
Please contact me if you have any questions or would like a re-focused search.

David

Search and Information Resources Administration

STIC EIC 2100
Search Request Form

Today's Date: 4-5-04

What date would you like to use to limit the search?
Priority Date: 7/06/01 Other:

Name John Tabone

AU 2135 Examiner # _____

Room # 6B05 Phone 305-8915

Serial # 09/876753

Format for Search Results (Circle One):
PAPER DISK EMAIL

Where have you searched so far?
USP DWPI EPO JPO ACM IBM TDB
IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

scan test system

2nd signature

2nd frequency

Masking

Reference signature

STIC Searcher Holloway Phone 308-7794

Date picked up 5-4-04 / Date Completed 5-5-04

DIALOG
$589.12/100
76 min

ip.com Prior Art Database

Search results

Publish ...
- a DEMO disclosure

Search/browse ...
- by full text
- by concept
- by document ID
- recent disclosures

Manage my ...
- account info
- events

View my ...
- prior purchases
- disclosures

Misc ...
- help and information
- main page
- about IP.com
- logout

Displaying records #1 through 22 out of 22

Result # 1 **Relevance:** ○○○○○

PREVIEW this document

BI-MODALLY SHIFTABLE SCAN CHAIN

19-Jun-2003 IPCOM000014236D English (United States)

Title: Bi-modally Shiftable Scan Chain Problem: Scan based designs depend on serially loading and unloading the system latches or Shift Register Latches (SRLs) to support the structural test methodology and interface with the logic within the device. When the scan ...

Result # 2 **Relevance:** ○○○○

PREVIEW this document

LAYOUT SCAN INSERTION AND SCHEMATIC BACKANNOTATION FOR AT SPEED TEST

16-Apr-2002 IPCOM000007698D English (United States)

A full-scan microprocessor architecture requires connecting every flip-flop in the design together into a serial shill register by daisy chaining the scan data output of one flip-flop (SDO) to the scan data input (SDI) of the next flip-flop. These connections make up the ...

Result # 3 **Relevance:** ○○○

PREVIEW this document

DC Scan Diagnostic Method

17-Feb-2004 IPCOM000021956D English (United States)

This article proposes a solution to the problem of testing and efficiently diagnosing DC (broken or stuck-at) scan chain defects and localizing these defects to a failing Shift Register Latch (SRL) or associated scan clock tree. This on-the-fly quick and accurate ...

Result # 4 **Relevance:** ○○○

PREVIEW this document

Method and apparatus for reducing logic activity during high-speed scan chain operation

25-Mar-2004 IPCOM000022689D English (United States)

Disclosed is a method and apparatus for reducing logic activity during high-speed scan chain

```
Set     Items   Descripti
S1       2280   SCAN()(CHAIN? OR STRING?) OR SIGNATURE()ANALY?
S2    2426442   FAULT? OR FLAW? OR ERROR? OR CORRUPT? OR BAD
S3    1057223   MASK? OR HIDE? OR OVERWRIT? OR OVER()RID? OR OVERRID? OR I-
            GNOR?
S4      11975   SIGNATURE(2N)(REFERENC? OR GOLDEN OR BASE? OR ORIGINAL? OR
            FIRST? OR INITIAL?)
S5      14029   (SECOND OR ADDITIONAL OR 2ND OR NEW OR TWO)(2N)SIGNATURE?
S6      19095   (SECOND OR 2ND OR ADDITIONAL? OR DIFFERENT?)(2N)(FREQ OR F-
            REQUENC?)
S7        371   S1(S)S2
S8          4   S7(S)S3
S9          0   S1(S)(S4 OR S5)(S)S6
S10         8   S1(S)S6(S)(S2 OR S3)
S11        16   S7(S)(S3 OR ALIAS?)
S12        24   S8 OR S10 OR S11
S13        22   RD (unique items)
S14        20   S13 NOT PY>2001
S15        20   S14 NOT PD=20010706:20030706
S16        20   S15 NOT PD=20030706:20040509
File 275:Gale Group Computer DB(TM) 1983-2004/May 05
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/May 05
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/May 05
         (c) 2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/May 04
         (c) 2004 McGraw-Hill Co. Inc
File 484:Periodical Abs Plustext 1986-2004/Apr W4
         (c) 2004 ProQuest
File 613:PR Newswire 1999-2004/May 05
         (c) 2004 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 141:Readers Guide 1983-2004/May
         (c) 2004 The HW Wilson Co
File 696:DIALOG Telecom. Newsletters 1995-2004/May 04
         (c) 2004 The Dialog Corp.
File 621:Gale Group New Prod.Annou.(R) 1985-2004/May 04
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Apr W4
         (c) 2004 IDG Communications
File 369:New Scientist 1994-2004/Apr W4
         (c) 2004 Reed Business Information Ltd.
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File  15:ABI/Inform(R) 1971-2004/May 04
         (c) 2004 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2004/May 04
         (c) 2004  The Gale Group
File  13:BAMP 2004/Apr W4
         (c) 2004  The Gale Group
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2004/May 05
         (c) 2004 Business Wire.
File 647:CMP  Computer Fulltext 1988-2004/Apr W4
         (c) 2004 CMP Media, LLC
File 148:Gale Group Trade & Industry DB 1976-2004/May 05
         (c)2004 The Gale Group
```

16/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01562898 SUPPLIER NUMBER: 14206796
Synopsys taps Bell Northern for BIST; will integrate the methodology into its test-synthesis suite. (built-in self-test)
Runyon, Stan
Electronic Engineering Times, n757, p8(1)
August 2, 1993
ISSN: 0192-1541 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

...ABSTRACT: The technology enables the functional circuits of ASICs to run at full design speeds. A **fault** simulator in BNR's version runs stuck-at and transition- **fault** tests on combinational circuits. Only such at-speed testing is capable of discovering hidden design or manufacturing problems. ScanBist, which is based on full scan and boundary scan, handles multiple **scan chains** at **different** clock **frequencies** . Synopsys plans to improve on the BNR approach.

16/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01472088 SUPPLIER NUMBER: 12907536
Performance of signature registers in the presence of correlated errors. (Technical)
Edirisooriya, G.; Robinson, J.P.
IEE Proceedings Part E Computers and Digital Techniques, v139, n5, p393(8) Sept, 1992
DOCUMENT TYPE: Technical ISSN: 0143-7062 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: In **signature analysis**, **aliasing** is usually examined under the independent or the q-ary symmetric **error** model. In contrast to the independent **error** model, the q-ary **error** model assumes space correlation among outputs. However, both independent and q-ary **error** models assume that the **errors** resulting from consecutive test vectors are independent over time. This assumption is reasonable for combinational...

...the previous state as well as the current input vector. For this reason a new **error** model, called the generalised time dependent q-ary (GTDQ) **error** model, is proposed. This **error** model extends the q-ary **error** model to consider both space and time correlation. A second parameter c is used to model the time correlation. By modeling the **signature analyser** as a Markov process the authors obtain a closed form expression for exact **aliasing** probability for arbitrary test length for a class of multiple -input linear automata signature registers...

...category. Finally, experimental results are provided for some real sequential circuits to validate the proposed **error** models. (Reprinted by permission of the publisher.)

16/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01402044 SUPPLIER NUMBER: 11323187
Analysis of detection capability of parallel signature analyzers. (includes an appendix with proofs of theorems)
Yinghua Min; Malaiya, Yashwant K.; Boping Jin
IEEE Transactions on Computers, v40, n9, p1075(7)
Sept, 1991
ISSN: 0018-9340 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

ABSTRACT: A deterministic approach to error **aliasing** in parallel **signature analyzers** (PSA) results in a two-signature scheme for providing complete **aliasing** double **error** coverage. Sixteen-bit PSAs, which compress 15 times the information of 16-bit serial **signature analyzers** , are liable to **aliasing** double **errors** wherein two single **errors** created during the signature formation cause **aliasing** . The **errors** ' components may occur during different clock periods and, even if more bits are added in the PSA, **aliasing** double **error** cannot be avoided. An analysis shows the necessary and sufficient conditions for four PSAs under which an **error** pattern results in **aliasing** . Double **errors** , significant for PSAs, are found to be disjointed. A reconfigurable design requiring two signatures can detect all possible double **errors** in PSAs.

16/3,K/12 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01227233 SUPPLIER NUMBER: 07153363
Comparative analysis of different implementations of multiple-input signature analyzers. (technical)
Maxwell, Peter C.
IEEE Transactions on Computers, v37, n11, p1411(4)
Nov, 1988
DOCUMENT TYPE: technical ISSN: 0018-9340 LANGUAGE: ENGLISH
RECORD TYPE: ABSTRACT

ABSTRACT: **Signature analysis** is an approved method of obtaining data compression for built-in testing applications. A unified approach to the analysis of multiple-input **signature analyzers** is given and involves considering them as finite state switching circuits. This approach is utilized...

...of alternatives to achieve a given polynomial. The approach also provides a method of expressing **aliasing** patterns for both implementations, leading to a study of the differences with regard to certain **error** detection capabilities.

16/3,K/14 (Item 1 fr[redacted] file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02721814 Supplier Number: 43639622 (USE FORMAT 7 FOR FULLTEXT)
Designing for test is beginning to reach the system level: CONVENTIONAL IN-CIRCUIT AND FUNCTIONAL-TESTING TECHNIQUES NO LONGER SUFFICE
Electronic World News, p12
Feb 8, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2301

... developed a proprietary technique, called ScanBist, that appears to overcome the problems encountered when multiple **scan chains** must be clocked at **different frequencies** - a typical telecommunications problem. The major benefit of ScanBist is that circuits can be tested at speed, a capability not usually associated with scan testing. Thus, a **fault** simulator can run exhaustive stuck-at and transition- **fault** tests on combinational circuits.

How it works

In operation, the technique synchronizes the multiple chains...

16/3,K/15 (Item 2 fr[redacted]file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02678848 Supplier Number: 43574207 (USE FORMAT 7 FOR FULLTEXT)
DESIGNERS BUILD IN SYSTEM-LEVEL TESTABILITY, OVERCOME LACK TO TOOLS: Design-for-test finally comes a-board
Electronic Engineering Times, p39
Jan 11, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3078

... developed a proprietary technique, called ScanBist, that appears to overcome the problems encountered when multiple **scan chains** must be clocked at **different frequencies** - a typical telecommunications problem. The major benefit of ScanBist is that circuits can be tested at speed, a capability not usually associated with scan testing. Thus, a **fault** simulator can run exhaustive stuck-at and transition- **fault** tests on combinational circuits.

In operation, the technique synchronizes the multiple chains, one of which...

16/3,K/19 (Item 1 fr[redacted] file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08011492 SUPPLIER NUMBER: 17156000 (USE FORMAT 7 OR 9 FOR FULL TEXT)
LogicVision picks up the BIST beat. (LogicVision's ICBIST CAD software) (built-in self-test) (Design Automation Conference '95 Preview) (Product Announcement)
Runyon, Stan
Electronic Engineering Times, n851, p62(1)
June 5, 1995
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 733 LINE COUNT: 00062

...ABSTRACT: operate with more than one system clock. LogicBIST operates the chains at up to three **different frequencies** at one time; it provides exact **fault** -coverage information rather than **fault** samples. ICBIST costs from $140,000 per seat.

```
Set     Items   Description
S1       5115   SCAN()(CHAIN? OR STRING?) OR SIGNATURE()ANALY?
S2    1642437   FAULT? OR FLAW? OR ERROR? OR CORRUPT? OR BAD
S3     280713   MASK? OR HIDE? OR OVERWRIT? OR OVER()RID? OR OVERRID? OR I-
              GNOR?
S4       3542   SIGNATURE(2N)(REFERENC? OR GOLDEN OR BASE? OR ORIGINAL? OR
              FIRST? OR INITIAL?)
S5       3728   (SECOND OR ADDITIONAL OR 2ND OR NEW OR TWO)(2N)SIGNATURE?
S6      54939   (SECOND OR 2ND OR ADDITIONAL? OR DIFFERENT?)(2N)(FREQ OR F-
              REQUENC?)
S7         55   S1 AND S2 AND S3 AND SIGNATURE?
S8        403   S1 AND (S4 OR S5)
S9          3   S8 AND S6
S10         7   S8 AND S3
S11        58   S7 OR S9 OR S10
S12        33   RD (unique items)
S13        29   S12 NOT PY>2001
S14        29   S13 NOT PD>20010706
File   8:Ei Compendex(R) 1970-2004/Apr W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Apr
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/May W1
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Apr W4
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Apr W2
         (c)2004 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/May 05
         (c) 2004 The Gale Group
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File   6:NTIS 1964-2004/May W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Apr W4
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W4
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
         (c) 2004 The HW Wilson Co.
```

14/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04359434 E.I. No: EIP96033067200
Title: Error masking **in compact testing based on the hamming code and its modifications**
Author: Demidenko, Serge; Ivanyukovich, Alexander; Makhist, Leonid; Piuri, Vincenzo
Corporate Source: Singapore Polytechnic, Singapore, Singapore
Conference Title: Proceedings of the 1995 4th Asian Test Symposium
Conference Location: Bangalore, India Conference Date: 19951123-19951124
Sponsor: IEEE; VLSI
E.I. Conference No.: 44382
Source: Proceedings of the Asian Test Symposium 1995. IEEE, Los Alamitos, CA, USA,95CS8084. p 303-307
Publication Year: 1995
CODEN: 001062
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9605W1
Abstract: Probability that an invalid sequence at an output of a device under test is not detected(**error masking**) is the measure of the effectiveness of compact testing methods. This paper evaluates and analyses the probability distribution of **error masking** for compact testing by exploiting the characteristics both of the Hamming code (i.e., the **signature analysis**) and of some modified Hamming codes. To study the effectiveness of these methods, we derive also the analytical expressions for the number of code words of arbitrary weight. Finally, bounds for **error masking** probability are obtained. (Author abstract) 8 Refs.
Descriptors: Integrated circuit testing; Probability; **Errors** ; Codes (symbols); Polynomials; Functions; Circuit theory
Identifiers: **Error masking** ; Compact testing; Hamming code; Prange theorem
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 922.1 (Probability Theory); 723.2 (Data Processing); 921.1 (Algebra); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 703.1 (Electric Networks)
714 (Electronic Components); 922 (Statistical Methods); 723 (Computer Software); 921 (Applied Mathematics); 721 (Computer Circuits & Logic Elements); 703 (Electric Circuits)
71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING)

14/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03769249 E.I. No: EIP93121153544
Title: Monitoring BIST by covers
Author: Gossel, M.; Jurgesnsen, H.
Corporate Source: Univ fo Postdam, Mahlow, Ger
Conference Title: Proceedings of the European Design Automation Conference
Conference Location: Hamburg, Ger Conference Date: 19930920-19930924
Sponsor: Gesellschaft fur Informatik e.V.; IEEE Computer Society; IEEE Circuits & Systems Society; ACM SIGDA; IFIP 10.5; EDAC
E.I. Conference No.: 19518
Source: 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 208-213
Publication Year: 1993
ISBN: 0-8186-4352-8
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental)
Journal Announcement: 9402W2
Abstract: We show how to combine a conventional built-in self-test method with a simple method for on-line **error** detection for combinational circuits. The output sequence of one or more components of the **signature analyzer** is monitored, in test mode, by an **error** detection circuit consisting of a 1-cover and a 0-cover. The cover circuits need to detect only such **faults** that are **masked** by the **signature analyzer** . Because of a large number of don't care conditions for the cover circuits the hardware overhead is very low. All **faults** in the **fault** model under considerations are detected either by the cover circuits or, due to an erroneous **signature** , by the **signature analyzer** . (Author abstract) 10 Refs.
Descriptors: *Integrated circuit testing; Combinatorial circuits
Identifiers: Built-in self-test (BIST); **Error** detection circuits; Linear feedback shift registers; Multiple input **signature analyzer** (MISA); Test input generator (TIG)
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 721.2 (Logic Elements); 721.3 (Computer Circuits)
714 (Electronic Components); 721 (Computer Circuits & Logic Elements)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

14/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02805193 E.I. Monthly No: EIM8910-034413
Title: Design of self-diagnostic boards by signature analysis .
Author: Karpovski, Mark G.; Nagvajara, Prawat
Corporate Source: Boston Univ, Dep of Electr, Comput & Syst Eng, MA, USA
Source: IEEE Transactions on Industrial Electronics v n M 1989. p 241-245
CODEN: ITIED6 ISSN: 0278-0046
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 8910
Abstract: The authors present a single- **faulty** -chip diagnostic technique which requires only **two** reference **signatures** for any number of chips on the original board. With this technique, it is possible to reduce substantially the hardware overhead compared to the diagnostic technique based on separate testing of each chip on the board. The technique can be also used for identification of **faulty** printed boards in a system or for identification of **faulty** processors in a multiprocessor system. 13 refs.
Descriptors: *INTEGRATED CIRCUIT TESTING; PRINTED CIRCUITS--Testing; PROBABILITY
Identifiers: SELF-DIAGNOSTIC BOARDS; **SIGNATURE ANALYSIS** ; DESIGN FOR TESTABILITY; PC BOARD TESTING; **ERROR MASKING** PROBABILITIES
Classification Codes:
713 (Electronic Circuits); 714 (Electronic Components); 922 (Statistical Methods)
71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

14/5/7 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02550300 E.I. Monthly No: EIM8803-012355

Title: OPTIMAL TIME AND SPACE COMPRESSION OF TEST RESPONSES FOR VLSI DESIGNS.

Author: Karpovsky, M.; Nagvajara, P.
Corporate Source: Boston Univ, MA, USA

Conference Title: International Test Conference 1987 - Proceedings: Integration of Test With Design and Manufacturing.
Conference Location: Washington, DC, USA Conference Date: 19870901
Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA; IEEE, Philadelphia Section, Philadelphia, PA, USA
E.I. Conference No.: 10689
Source: Digest of Papers - International Test Conference 1987. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 87CH2437-2), Piscataway, NJ, USA p 523-529
Publication Year: 1987
CODEN: DITCDP ISSN: 0743-1686 ISBN: 0-8186-0798-X
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8803

Abstract: A technique for optimal test response compression is presented. With the assumption that a **fault** -free response is uniformly distributed, the proposed quadratic compression scheme is shown to be optimal with respect to the total **error - masking** probability, the maximum value of the conditional **error - masking** probability given an **error** sequence, and the maximum value of the conditional **error - masking** probability given a **fault** -free sequence. An implementation of the quadratic compression scheme requires slightly more hardware than a parallel **signature analyzer** by linear-feedback shift registers. The advantage of a quadratic compression technique over linear compression techniques is that the conditional **error - masking** probability is constant, given an **error** sequence, for a quadratic scheme, which implies equal protection against all **error** patterns. Thus the quadratic compression technique is robust with respect to a statistics of **error** patterns. 9 refs.

Descriptors: INTEGRATED CIRCUITS, VLSI--*Testing; CODES, SYMBOLIC-- **Error** Detection; AUTOMATIC TESTING--Mathematical Models; PROBABILITY
Identifiers: OPTIMAL TIME AND SPACE COMPRESSION; TEST RESPONSES; **ERROR - MASKING** PROBABILITY; QUADRATIC COMPRESSION TECHNIQUE
Classification Codes:
713 (Electronic Circuits); 714 (Electronic Components); 723 (Computer Software); 922 (Statistical Methods)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

14/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02108681 E.I. Monthly No: EIM8608-051250
Title: ISOLATING FAILURES WITHIN VLSI CHIPS THAT INCORPORATE SIGNATURE ANALYSIS **AND SET/SCAN TECHNIQUES.**
Author: Koo, Frances D.; Lee, Gene W.
Corporate Source: Hughes Aircraft Co, El Segundo, CA, USA
Conference Title: International Test Conference, 1985 Proceedings: The Future of Test.
Conference Location: Philadelphia, PA, USA Conference Date: 19851119
Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA; IEEE, Philadelphia Section, Philadelphia, PA, USA
E.I. Conference No.: 08028
Source: Digest of Papers - International Test Conference 1985. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 85CH2230-1), Piscataway, NJ, USA p 372-377
Publication Year: 1985
CODEN: DITCDP ISSN: 0743-1686 ISBN: 0-8186-0641-X
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8608
Abstract: The difficulty of **fault** location is a function of circuit complexity and configuration. A diagnosis algorithm has been developed and automated to obtain a **fault** -set, by guiding the test engineer through a debug procedure to gather test data for **fault** diagnosis. This procedure incorporates **signature analysis** and set/scan techniques to deduce the **fault** -set. A specialized piece of **signature** generation hardware has been designed to take advantage of exhaustively testable partitions. The need for guesswork, custom test procedures, or intimate knowledge of the circuit are eliminated. Except in cases where the **fault** has been **masked** during **signature** compression, this **fault** -location procedure permits location of all detected single stuck-at failures that do not introduce new states. 14 refs.
Descriptors: *LOGIC CIRCUITS--*Automatic Testing; INTEGRATED CIRCUITS, VLSI
Identifiers: LOGIC CIRCUIT **FAULT** DIAGNOSIS; **SIGNATURE ANALYSIS** ; VLSI CHIPS
Classification Codes:
721 (Computer Circuits & Logic Elements); 723 (Computer Software); 713 (Electronic Circuits); 714 (Electronic Components)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

14/5/11 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02089570 E.I. Monthly No: EIM8605-027870
Title: ENHANCING THE EFFECTIVENESS OF PARALLEL SIGNATURE ANALYZERS .
Author: Hassan, Syed Zahoor; McCluskey, Edward J.
Corporate Source: Stanford Univ, CA, USA
Conference Title: Digest of Technical Papers - IEEE International Conference on Computer-Aided Design, ICCAD-84.
Conference Location: Santa Clara, CA, USA Conference Date: 19841112
Sponsor: IEEE Computer Soc, Los Alamitos, CA, USA; IEEE Circuits & Systems Soc, New York, NY, USA; IEEE Electron Devices Soc, New York, NY, USA
E.I. Conference No.: 07818
Source: Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 84CH2026-3), Piscataway, NJ, USA p 102-104
Publication Year: 1984
ISBN: 0-8186-607-X
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8605
Abstract: A scheme for enhancing the **fault** coverage of **signature** testing for multiple output circuits is presented. The increased coverage is obtained by reducing the frequencies of aliasing thorough use of **two signatures** . The test time is increased by a factor of two. The extra hardware needed for this scheme is relatively small. The problem of **fault masking** is also analyzed. It is shown that the frequency of **fault masking** can be substantially reduced by obtaining a third **signature** corresponding to the reverse order of input patterns and the original order of CUT output connections to the **signature analyzers** . The proposed multiple **signature** scheme can be used in conjunction with any kind of test pattern (for example, test patterns generated to cover all single stuck-at **faults**). 12 refs.
Descriptors: *LOGIC CIRCUITS--*Testing; INTEGRATED CIRCUIT TESTING; COMPUTER AIDED DESIGN
Identifiers: PARALLEL **SIGNATURE ANALYZERS** ; **FAULT** COVERAGE; LOGIC CIRCUIT **FAULT** DIAGNOSIS; MULTIPLE-OUTPUT CIRCUITS; **SIGNATURE** TESTING
Classification Codes:
721 (Computer Circuits & Logic Elements); 714 (Electronic Components); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

14/5/15 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4488378 INSPEC Abstract Number: B9311-1265B-036, C9311-5210-014
Title: Multiple signature analysis : a framework for built-in self-diagnostic
Author(s): Karpovsky, M.G.; Chaudhry, S.M.; Levitin, L.B.
Author Affiliation: Dept. of Electr. Comput. & Syst. Eng., Boston Univ., MA, USA
Conference Title: Digest of Papers. The 1992 IEEE Workshop on Fault-Tolerant Parallel and Distributed Systems (Cat. No.92TH0449-9) p. 112-19
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1992 Country of Publication: USA viii+233 pp.
ISBN: 0 8186 2870 7
U.S. Copyright Clearance Center Code: 0 8186 2870 7/92$03.00
Conference Sponsor: IEEE
Conference Date: 6-7 July 1992 Conference Location: Amherst, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A framework, based on nonbinary multiple **error** correcting codes for built-in self-diagnostic is presented. New space-time compressors are proposed for test response compression and **fault** diagnosis. **Fault** -detecting and locating capabilities for space-time compressors are analyzed in the case when nonbinary Reed-Solomon codes are used and **fault** - **masking** and diagnosis probabilities for the chip-independent **error** model are estimated. For this **error** -model, the **fault** - **masking** probabilities are analyzed using the weight distributions of Reed-Solomon codes. (20 Refs)
Subfile: B C
Descriptors: built-in self test; **error** correction codes; logic testing; Reed-Solomon codes
Identifiers: multiple **signature analysis** ; framework; built-in self-diagnostic; nonbinary multiple **error** correcting codes; space-time compressors; test response compression; **fault** diagnosis; nonbinary Reed-Solomon codes; **fault - masking** ; diagnosis probabilities; chip-independent **error** model; **error** -model; weight distributions
Class Codes: B1265B (Logic circuits); B0170E (Production facilities and engineering); B7210B (Automatic test and measurement systems); B6120B (Codes); C5210 (Logic design methods)

14/5/18 (Item 4 from [redacted]le: 2)
DIALOG(R)File 2:INSPEC

03513430 INSPEC Abstract Number: B89075104, C90001826
Title: Fault masking **probabilities with single and multiple** signature analysis
Author(s): Doenhardt, J.
Author Affiliation: Univ.-Gesamthochschule-Paderborn, West Germany
Conference Title: STACS 89. 6th Annual Symposium on Theoretical Aspects of Computer Science. Proceedings p.327-38
Editor(s): Monien, B.; Cori, R.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1989 Country of Publication: West Germany viii+543 pp.
ISBN: 3 540 50840 6
Conference Date: 16-18 Feb. 1989 Conference Location: Paderborn, West Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Given a circuit output sequence fed into a d-bit **signature analyzer** , the author investigates the probability that a **faulty** output sequence is **masked** , i.e. that its **signature** and the **signature** of the correct sequence are the same. If all possible **faulty** output sequences are assumed to be equally likely, it is known that the probability comes close to 2/sup -d/. It is restricted to **faulty** output sequences having exactly z **faults** , z fixed. Small values of z are of practical interest, because they correspond to failures that are hard to detect by most of other circuit testing methods. Using the theory of **error** -correcting codes, formulas for the **masking** probability of such sequences are derived. It is shown that, especially for small z, this probability can be much greater than 2/sup -d/, and that it is not only dependent on the length of the **signature analysis** register. The paper is also concerned with multiple **signature analysis** using more than one **signature** register. (7 Refs)
Subfile: B C
Descriptors: **error** correction codes; **fault** location; logic testing
Identifiers: **fault masking** probabilities; **signature analysis** ; circuit output sequence; d-bit **signature analyzer** ; probability; **faulty** output sequence; circuit testing methods; **error** -correcting codes
Class Codes: B1265B (Logic circuits); B6120B (Codes); C5210 (Logic design methods)

14/5/27 (Item 2 from [redacted]le: 144)
DIALOG(R)File 144:Pascal

08698045 PASCAL No.: 89-0247302
Error **cancellation in multiple-input** signature **registeres**
JOURNEAU M; MCANNEY W H
Cie IBM France, Montpellier 34006, France
Journal: Automatique, productique, informatique industrielle, 1988, 22 (6) 597-605
ISSN: 519340 CODEN: RAPIEK Availability: CNRS-9323D
No. of Refs.: 2 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: France
Language: English Summary Language: French

English Descriptors: Shift register; Multientry; **Error** correction; Reliability; **Signature analysis** ; Test; **Masking**

French Descriptors: Registre decalage; Entree multiple; Correction erreur; Fiabilite; Analyse **signature** ; Test; Masquage

Classification Codes: 250A10I; 001D03J09

```
Set     Items   Descripti
S1      38534   SCAN()CHAIN? OR SIGNATURE()ANALY? OR SHIFT()REGISTER?
S2     486683   FAULT? OR FLAW? OR ERROR? OR CORRUPT? OR BAD
S3     241169   MASK? OR HIDE? OR OVERWRIT? OR OVER()RID? OR OVERRID? OR I-
            GNOR?
S4        826   SIGNATURE(2N)(REFERENC? OR GOLDEN OR BASE? OR ORIGINAL? OR
            FIRST? OR INITIAL?)
S5        507   (SECOND OR ADDITIONAL OR 2ND OR NEW OR TWO)(2N)SIGNATURE?
S6         61   S1 AND S2 AND S3
S7          3   S6 AND (S4 OR S5)
S8        791   BIST OR BUILT()IN()SELF()TEST? OR LBIST?
S9      38696   (SECOND OR 2ND OR ADDITIONAL? OR DIFFERENT?)(2N)(FREQ OR F-
            REQUENC?)
S10        12   (S1 OR S8) AND S2 AND S3 AND SIGNATUR?
S11       280   (S1 OR S8) AND S9
S12         1   S11 AND S3
S13        17   (S1 OR S8) AND S3 AND SIGNATUR?
S14        18   S7 OR S10 OR S12 OR S13
S15        13   S14 AND IC=G06F?
S16        18   S6 AND IC=G06F-011?
S17        10   S16 NOT S14
S18       435   SCAN()(CHAIN? OR STRING?)
S19         2   S18 AND S2 AND S3 AND SIGNATUR?
File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200427
         (c) 2004  Thomson Derwent
```

15/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011344487 **Image available**
WPI Acc No: 1997-322392/199730
XRPX Acc No: N97-266755

Boundary-scan testing method for testing system having chain of serially-connected boundary-scan cells - in which filtered system response to test pattern is compared to reference set of bits representing fault -free condition

Patent Assignee: AT & T CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: KE W
Number of Countries: 010 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 780767	A2	19970625	EP 96309111	A	19961213	199730	B
JP 9189749	A	19970722	JP 96336195	A	19961217	199739	
CA 2192867	A	19970623	CA 2192867	A	19961213	199743	
US 5774477	A	19980630	US 95577454	A	19951222	199833	
TW 343321	A	19981021	TW 96113948	A	19961114	199909	

Priority Applications (No Type Date): US 95577454 A 19951222
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 780767	A2	E	10	G06F-011/267	
Designated States (Regional): DE FR GB IT NL SE					
JP 9189749	A		8	G01R-031/28	
CA 2192867	A			G01R-031/28	
US 5774477	A			G01R-031/28	
TW 343321	A			G06T-009/20	

Abstract (Basic): EP 780767 A

The pseudorandom boundary-scan testing method for testing interconnects within a system (10) involves generating a pseudorandom pattern and filtering the pattern before application to the system to modify values within each pattern that could cause a signal conflict.

Each response generated by the system upon application to the system is also filtered to **mask** non-deterministic values within the response. The filtered response is compared to a set of **signatures** representing a **fault** -free condition to detect **faults** within the system.

USE/ADVANTAGE - Applying pseudo-random patterns to test interconnects in boundary scan environment. Can be practised for several different **scan chains** simultaneously such that interconnects surrounded by each chain will be tested at same time.

Dwg.1/4

Title Terms: BOUNDARY; SCAN; TEST; METHOD; TEST; SYSTEM; CHAIN; SERIAL; CONNECT; BOUNDARY; SCAN; CELL; FILTER; SYSTEM; RESPOND; TEST; PATTERN; COMPARE; REFERENCE; SET; BIT; REPRESENT; **FAULT** ; FREE; CONDITION
Derwent Class: T01
International Patent Class (Main): G01R-031/28; **G06F-011/267** ; G06T-009/20
International Patent Class (Additional): **G06F-011/22** ; **G06F-011/27**
File Segment: EPI

```
Set     Items   Description
S1        911   SCAN()(CHAIN? OR STRING?) OR SIGNATURE()ANALY?
S2     258297   FAULT? OR FLAW? OR ERROR? OR CORRUPT? OR BAD
S3     196105   MASK? OR HIDE? OR OVERWRIT? OR OVER()RID? OR OVERRID? OR I-
             GNOR?
S4       2585   SIGNATURE(2N)(REFERENC? OR GOLDEN OR BASE? OR ORIGINAL? OR
             FIRST? OR INITIAL?)
S5       2063   (SECOND OR ADDITIONAL OR 2ND OR NEW OR TWO)(2N)SIGNATURE?
S6      44695   (SECOND OR 2ND OR ADDITIONAL? OR DIFFERENT?)(2N)(FREQ OR F-
             REQUENC?)
S7          1   S1(S)S2(S)S3(S)(S4 OR S5)
S8          6   S1(S)S2(S)S3(S)SIGNATURE?
S9         71   S1(S)(S4 OR S5)
S10        18   S9 AND IC=G06F-011?
S11        23   S7 OR S8 OR S10
S12        16   S11 NOT AD>20010706
S13        16   IDPAT (sorted in duplicate/non-duplicate order)
S14        15   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2004/Apr W04
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040415,UT=20040408
         (c) 2004 WIPO/Univentio
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14/3,K/3 (Item 3 fro[redacted]ile: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00480045
Built-in self-test technique for read-only memories
Technik zum eingebauten Selbsttest fur Nur-Lese-Speicher
Technique pour auto-test integre pour memoires mortes
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Zorian, Yervant, 31B Chicopee Drive, Princetown, New Jersey 08540, (US)
LEGAL REPRESENTATIVE:
Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 441518 A2 910814 (Basic)
EP 441518 A3 920701
EP 441518 B1 960904
APPLICATION (CC, No, Date): EP 91300663 910129;
PRIORITY (CC, No, Date): US 475524 900206
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: G11C-029/00; **G06F-011/26**
ABSTRACT WORD COUNT: 205
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

US 5,091,908

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1240
CLAIMS B	(English)	EPAB96	1259
CLAIMS B	(German)	EPAB96	1321
CLAIMS B	(French)	EPAB96	1442
SPEC A	(English)	EPABF1	5826
SPEC B	(English)	EPAB96	5904
Total word count - document A			7066
Total word count - document B			9926
Total word count - documents A + B			16992

...INTERNATIONAL PATENT CLASS: **G06F-011/26**

...SPECIFICATION determination can be made as to whether the ROM Is faulty.

The advantage of the **signature analysis** technique for self-testing of a ROM is that the residue which remains in the MISR (representing the " **signature** " of the ROM) is only n bits long. Thus, by using **signature analysis** , the m x n bits of data stored in the ROM are effectively condensed or compacted into an n bit string. Consequently, if all possible **error** patterns are assumed to be equally likely, the possibility of **error** escape is 2(sup(-)(sup(n). Although the likelihood of **error** escape using the conventional **signature analysis** may seem small, even a small likelihood of **error** is undesirable for high quality **fault** coverage. The **error** escape which occurs during conventional **signature analysis** is attributable to **error masking** and **error** cancellation. **Error** cancellation can occur each time each of a successive row of bits of the ROM...

...OR'd in this manner are thus diagonally adjacent, and if each is erroneous, the **errors** tend to cancel each other out during the polynomial division. Consequently, the residue remaining in...

...MISR may not reflect the presence of an even number of erroneous, diagonally adjacent bits. **Error masking** arises from the compaction of the m x n-1 string into the n bit...

...process. Failure to map one or more erroneous bits may give rise to an undetected **error** .
Therefore, there is a need for a self-test technique for a ROM which affords...residue means that none of the errors in the ROM 10' are lost (masked) during **signature analysis** .

Referring to FIG. 3, [redacted]lowing the completion of the s[redacted]nd polynomial division during step 32...

...SPECIFICATION present), a determination can be made as to whether the ROM Is faulty.

Such a **signature analysis** technique for testing random access memories using a bidirectional MISR, is shown in the article...

...IEICE, vol.17, no.10, October 1988, Tokyo, Japan, p.1013-1022, with the Title " **Referenceless Signature** Testing Using Bi-Directional LFSR" by Fujiwara.

The advantage of the **signature analysis** technique for self-testing of a ROM is that the residue which remains in the MISR (representing the " **signature** " of the ROM) is only n bits long. Thus, by using **signature analysis** , the m x n bits of data stored in the ROM are effectively condensed or compacted into an n bit string. Consequently, if all possible **error** patterns are assumed to be equally likely, the possibility of **error** escape is 2(sup(-n). Although the likelihood of **error** escape using the conventional **signature analysis** may seem small, even a small likelihood of **error** is undersirable for high quality **fault** coverage. The **error** escape which occurs during conventional **signature analysis** is attributable to **error masking** and **error** cancellation. **Error** cancellation can occur each time each of a successive row of bits of the ROM...

...OR'd in this manner are thus diagonally adjacent, and if each is erroneous, the **errors** tend to cancel each other out during the polynomial division. Consequently, the residue remaining in...

...MISR may not reflect the presence of an even number of erroneous, diagonally adjacent bits. **Error masking** arises from the compaction of the m x n - 1 string into the n bit...

...process. Failure to map one or more erroneous bits may give rise to an undetected **error** .

Therefore, there is a need for a self-test technique for a ROM which affords...residue means that none of the errors in the ROM 10' are lost (masked) during **signature analysis** .

Referring to FIG. 3, following the completion of the second polynomial division during step 32...

14/3,K/4 (Item 4 fr[redacted]ile: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00460174
Reduced delay circuits for shift register latch scan strings
Schaltungen mit reduzierter Verzogerung fur Schieberegisterabtastkette
Circuits a retard reduit pour chaine de balayage a bascule de registre a decalage
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Bardell, Paul Harold, Jr., Wellington Drive, Carmel, New York 10512, (US)
McAnney, William Howard, RR No.1, Box 276, LaGrangeville, New York 12540, (US)
LEGAL REPRESENTATIVE:
Teufel, Fritz, Dipl.-Phys. et al (11855), IBM Deutschland Informationssysteme GmbH, Patentwesen und Urheberrecht, 70548 Stuttgart , (DE)
PATENT (CC, No, Kind, Date): EP 469238 A2 920205 (Basic)
EP 469238 A3 930120
EP 469238 B1 960710
APPLICATION (CC, No, Date): EP 91105934 910413;
PRIORITY (CC, No, Date): US 561399 900801
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-011/26**
ABSTRACT WORD COUNT: 75

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	179
CLAIMS B	(English)	EPAB96	195
CLAIMS B	(German)	EPAB96	164
CLAIMS B	(French)	EPAB96	233
SPEC A	(English)	EPABF1	3611
SPEC B	(English)	EPAB96	3939
Total word count - document A			3790
Total word count - document B			4531
Total word count - documents A + B			8321

INTERNATIONAL PATENT CLASS: **G06F-011/26**

...SPECIFICATION generating pseudo-random bit sequences to be supplied to a plurality of shift register latch **scan strings** . These **scan strings** are divided into a first set of **scan strings** containing only the SRLs associated with primary inputs, and a second disjoint set of **scan strings** containing only those SRLs not associated with primary inputs. The first and second set of shift register latch **scan strings** are supplied respectively to **first** and **second signature** registers which are operable to compress signals from the SRLs into separate signatures. Even more particularly, the shift register latches associated with the primary inputs (first set of **scan strings**) are constructed without delay-causing input degating.
Accordingly, it is an object of the present...

...SPECIFICATION generating pseudo-random bit sequences to be supplied to a plurality of shift register latch **scan strings** . These **scan strings** are divided into a first set of **scan strings** containing only the SRLs associated with primary inputs, and a second disjoint set of **scan strings** containing only those SRLs not associated with primary inputs. The first and second set of shift register latch **scan strings** are supplied respectively to **first** and **second signature** registers which are operable to compress signals from the SRLs into separate signatures. Even more particularly, the shift register latches associated with the primary inputs (first set of **scan strings**) are constructed without delay-causing input degating.

Accordingly, it is an object of the present...